What is claimed is:

1. A demodulator comprising:

a wobble signal processor configured to convert a waveform of a wobble signal, and to generate a clock and a reference value based on a converted wobble signal;

a sampling circuit configured to sample the converted wobble signal by using the clock, and to generate a sampled signal; and

a viterbi decoder configured to decode an auxiliary recording signal superposed on an optical disk by using the reference value and the sampled signal.

2. The demodulator of claim 1, wherein the wobble signal processor comprises:

a waveform converter configured to measure a cycle of the wobble signal, and to generate the converted wobble signal;

a reference generator configured to calculate a mean value of an amplitude of the converted wobble signal, and to generate first, second, and third reference values based on the mean value; and

a clock generator configured to generate the clock based on the converted wobble signal and the mean value.

3. The demodulator of claim 2, wherein the waveform converter comprises:

an amplitude discriminator configured to binarize the wobble signal, and to generate a binarized wobble signal;

a period measuring circuit configured to measure periods between edges of the binarized wobble signal based on a measurement clock; and

a low-pass filter configured to smooth the output of the period measuring circuit.

4. The demodulator of claim 2, wherein the reference generator comprises:

a mean value calculator configured to calculate the mean value; and

a frequency shift circuit configured to generate the first, second, and third reference values.

5. The demodulator of claim 3, wherein the clock generator comprises:

a comparator configured to compare the converted wobble signal with the mean value, and to generate a comparison signal; and

a PLL configured to multiply the comparison signal, and to generate the clock.

6. The demodulator of claim 4, wherein the frequency shift circuit comprises:

a first shift circuit configured to calculate the first reference value based on the mean value; and

a second shift circuit configured to calculate the third reference value based on the mean value.

7. The demodulator of claim 4, wherein the viterbi decoder comprises:

a branch metric circuit configured to generate first, second, and third squared errors based on the first, second, and third reference values;

a path metric circuit configured to calculate a survivor path based on the first, second, and third squared errors; and

a path memory circuit configured to store a code sequence in accordance with the survivor path, and to merge the code sequence as a biphase signal.

8. The demodulator of claim 7, wherein the branch metric circuit comprises:

a first subtracter configured to calculate an error between the sampled signal and the first reference value, and to generate a first error signal;

a second subtracter configured to calculate an error between the sampled signal and the second reference value, and to generate a second error signal;

a third subtracter configured to calculate an error between the sampled signal and the third reference value, and to generate a third error signal;

a first multiplier configured to square the first error signal;

a second multiplier configured to square the second error signal; and

a third multiplier configured to square the third error signal.

9. The demodulator of claim 1, wherein the wobble signal processor comprises:

a clock generator configured to generate a first clock and a second clock based on the wobble signal;

a waveform converter configured to convert the waveform of the wobble signal by equalizing the waveform; and

a reference generator configured to generate the reference value.

10. The demodulator of claim 9, wherein the clock generator comprises:

an amplitude discriminator configured to convert the wobble signal into binary code; and

a PLL configured to generate the first clock and the second clock.

11. The demodulator of claim 10, wherein trailing edges of the first clock are synchronized with leading edges of the binary code, and the first clock has a frequency double the frequency of the wobble signal.

12. The demodulator of claim 10, wherein phase of the second clock is synchronized with the phase of the binary code, and the second clock has a frequency equal to the frequency of the wobble signal.

13. The demodulator of claim 12, wherein the sampling circuit samples the converted wobble signal in synchronization with leading edges of the second clock.

14. The demodulator of claim 11, wherein the waveform converter comprises:

an A/D converter configured to convert the wobble signal into digital data in synchronization with leading edges of the first clock; and

a partial response filter configured to equalize a waveform of the digital data in synchronization with the first clock.

15. The demodulator of claim 14, wherein the reference generator comprises:

an absolute value calculator configure to calculate an absolute value of the digital data;

a mean value calculator configure to calculate a mean value of the absolute value; and

an amplifier configured to normalize the mean value to an mean value of the sampled signal.

16. The demodulator of claim 14, wherein the reference generator comprises:

an absolute value calculator configure to calculate an absolute value of the sampled signal; and

a mean value calculator configure to calculate a mean value of the absolute value.

17. The demodulator of claim 14, wherein the partial response filter comprises:

a first F/F configured to receive the digital data;

a second F/F configured to receive output of the first F/F;

a third F/F configured to receive output of the second F/F;

a first multiplier configured to multiply the digital data and logic value "1";

a second multiplier configured to multiply the output of the first F/F and logic value "-1";

a third multiplier configured to multiply the output of the second F/F and logic value "1";

a fourth multiplier configured to multiply the output of the third F/F and logic value "-1"; and

an adder configured to add outputs of the first, second, third, and fourth multipliers.

18. The demodulator of claim 9, wherein the viterbi decoder comprises:

a branch metric circuit configured to generate first, second, and third squared errors based on the reference value and the sampled signal;

a path metric circuit configured to calculate a survivor path based on the first, second, and third squared errors; and

a path memory circuit configured to store a code sequence in accordance with the survivor path, and to merge the code sequence as an ADIP signal.

19. A semiconductor integrated circuit comprising:

a wobble signal processor integrated on a semiconductor chip and configured to

convert a waveform of a wobble signal, and to generate a clock and a reference value based on a converted wobble signal;

a sampling circuit integrated on the semiconductor chip and configured to sample the converted wobble signal by using the clock, and to generate a sampled signal; and

a viterbi decoder integrated on the semiconductor chip and configured to decode an auxiliary recording signal superposed on an optical disk by using the reference value and the sampled signal.

20. An optical disk drive comprising:

a pickup configured to receive light reflected from an optical disk, the reflected light generated by irradiating a laser beam on the optical disk;

an RF amplifier configured to amplify a wobble signal generated by the pickup from the received light;

a demodulator configured to generate a reference value and a sampled signal based on the wobble signal, and to subject an auxiliary recording signal superposed on the optical disk to viterbi decoding by using the reference value and the sampled signal;

a servo controller configured to control an operation of the pickup;

a reproducing/recording signal processor configured to carry out signal processing for reproducing or recording with the pickup; and

a recording controller configured to control recording of a recording signal from the reproducing/recording signal processor onto the optical disk.